Amendments to the Specification

Please replace the paragraph beginning at page 12, line 1, which starts with "(2) Grow a thermally deposited", with the following amended paragraph:

(2) Grow a thermally deposited [[P+]] diffusion oxide, preferably SiO_2, on the P+ substrate 301 and pattern the oxide in the shape of mask A 600, to open two windows 601 and 602 for N+ diffusion. The larger the area of the two windows 601 and 602 in mask A 600, the lower is the resistance of the two avalanche diodes 103 and 105.

Please replace the paragraph beginning at page 12, line 13, which starts with "(4) Remove the thermally grown", with the following amended paragraph:

(4) Remove the thermally grown [[P+]] diffusion oxide that was grown in step two.

Please replace the paragraph beginning at page 12, line 18, which starts with "(6) Grow a P+ diffusion", with the following amended paragraph:

(6) Grow a [[P+]] diffusion oxide 325 on the N-EPI layer 305 and pattern the oxide in the shape of mask B 700 for P+ diffusion.

Please replace the paragraph beginning at page 12, line 23, which starts with "(8) Apply mask C", with the following amended paragraph:

(8) Apply mask C over the existing [[P+]] diffusion oxide. Mask C 800 has two windows 801 and 802. The larger the area of these windows 801 and 802, the greater is the current-carrying capability of the resulting avalanche diodes 103 and 105.

Please replace the paragraph beginning at page 12, line 26 and ending on page 13, line 3, which starts with "(9) Diffuse the N+ regions", with the following amended paragraph:

(9) Diffuse the N+ regions in the N-EPI layer 305 to form the N+ first diffused region 311 of the TVS device 101. The N+ first diffused region 311 is used to fix the breakdown voltage of the TVS device 101. The depth of the N+ first diffused region 311 is selected to produce a preselected breakdown voltage. A greater depth results in a higher breakdown voltage, which, in turn, results in a higher clamping voltage. At the same time, re-grow the thermally deposited [[P+]] diffusion oxide 325 and apply mask D 900 over the [[P+]] diffusion oxide. Mask D 900 has four windows 901-904.

Please replace the paragraph beginning at page 13, line 4, which starts with "(10) Diffuse the P+ second", with the following amended paragraph:

(10) Diffuse the P+ second diffused region 313 and P+ third diffused region 315 in both the N+ first diffused region 311 and in a region in the N-EPI layer 305 over the N+ buried layer 303 and adjacent to, but not in contact with, the N+ first diffused region. The P+ diffusion of this step is selected such that the breakdown voltage will be controlled to a given specification in the N+ first diffused region 311. The P+ third diffused region 315 (anode) on the N-EPI layer and the N-EPI layer 305 (cathode) form the first rectifier diode junction. The high resistivity of the N-EPI layer 305 and the small size of the junction of the first rectifier diode 104 are preselected to provide a specific low value of junction capacitance. The P+ second diffused region 313 (anode) on the N+ first diffused region 311, and the diffused N+ first region (cathode) form a first avalanche diode junction. The high doping level (and low resistivity) of the N+ first diffused region 311, which is required for the desired avalanche breakdown voltage, results in a high internal capacitance of the first avalanche diode 103. At the same time, re-grow the thermally deposited [[P+]] diffusion oxide 325 and apply mask E 1000 over the oxide. Mask E 1000 has four windows 1001-1004.

Please replace the one-line paragraph beginning on page 15, line 32, (within the LIST OF REFERENCE NUMERALS), with the following amended paragraph:

325 Thermally Deposited [[P+]] Diffusion Oxide